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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/255,777	02/23/1999	SHUNPEI YAMAZAKI	0756-1936	9041

7590 02/26/2004

SIXBEY FRIEDMAN LEEDOM & FERGUSON PC
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN, VA 22102

EXAMINER

BOOTH, RICHARD A

ART UNIT	PAPER NUMBER
	2812

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/255,777	YAMAZAKI ET AL.
Examiner	Art Unit	
Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 01 December 2003.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 12,13,15-19,21-24,26-43,46-58,60,61,65-71 and 75-96 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 12,13,15-19,21-24,26-43,46-58,60,61,65-71 and 75-96 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/1/03 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 12, 15, 17, 23, 26, 28, 34-36, 46, 48, 50, 75, 77, 79, 88, and 90-91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoshi et al., JP 04-139727 in view of Yamazaki, U.S. Patent 4,727,044 and further in view of Mukai, U.S. Patent 5,077,233.

Satoshi et al. shows the invention substantially as claimed including forming a semiconductor film 3 comprising amorphous silicon over an insulating surface; forming an insulating film 4 on said semiconductor film; crystallizing at least an entire channel

formation region of said semiconductor film by laser irradiation through said insulating film (see fig. 1(b)); removing said insulating film; forming a gate insulating film 5 on said semiconductor film after removing said insulating film; forming a gate electrode 6 on said gate insulating film; and forming source and drain regions (7,8) in said semiconductor film by ion doping (see figures and abstract).

Satoshi et al. fails to expressly disclose removing the insulating film by wet etching and forming source and drain regions by ion doping through the gate insulating film.

Yamazaki discloses forming source and drain regions (5s,5d) by ion doping through the gate insulating film 3 (see figs. 5A-5G and col. 8-line 6 to col. 9-line 33). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Satoshi et al. so as to form the source and drain regions by implanting through the gate insulating film because this is shown to be a suitable method of forming a source and drain region and the use of screen insulating films for implantation purposes has been shown to be beneficial in reducing damage to semiconductor surfaces.

Regarding removing an insulating film by wet etching, Mukai discloses the formation of an insulating film, irradiating through the layer, and removing the film by wet etching (see figures 4b-4f and col. 7-line 6 to col. 9-line 67). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Satoshi et al. modified by Yamazaki since this is shown to be a suitable method in which to remove insulating films.

With respect to forming two active matrix panels and then performing a cutting process, the examiner takes official notice that is a well known method in which to form liquid crystal display devices.

Claims 32, 53-54, 67, 69, 82, 85, 94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoshi et al., JP 04-139727 in view of Yamazaki, U.S. Patent 4,727,044 and further in view of Mukai, U.S. Patent 5,077,233 as applied to claims 12, 15, 17, 23, 26, 28, 34-36, 46, 48, 50, 75, 77, 79, 88, and 90-91 above, and further in view of Ito et al., "Thin Film Technology of VLSI", pages 87-88.

Satoshi et al., Yamazaki, and Mukai are applied as above but both references fail to expressly disclose forming the insulating film using TEOS.

Ito et al. discloses forming an oxide layer using TEOS (see abstract, section 3.3.3). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Satoshi et al. modified by Yamazaki and Mukai so as to form the oxide insulating film using a TEOS precursor because Ito et al. shows this to be a suitable method to form an oxide film.

Claims 18, 21-22, 27, 47, 76, and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoshi et al., JP 04-139727 in view of Yamazaki, U.S. Patent 4,727,044 and further in view of Mukai, U.S. Patent 5,077,233 as applied to claims 12, 15, 17, 23, 26, 28, 34-36, 46, 48, 50, 75, 77, 79, 88, and 90-91 above, and further in view of Han et al., U.S. Patent 4,599,118.

Satoshi et al., Yamazaki, and Mukai are applied as above but fail to expressly disclose forming a gate electrode having tapered side edges formed by wet etching and wherein said channel formation region between said source and drain region has a first length in contact with said gate insulating film and a second length at a surface in contact with said insulating surface, where said first length is shorter than said second length.

Han et al. discloses forming a gate electrode with tapered sides which will inherently lead to the channel structure claimed by applicant (see Figures 4-7 and col. 3-line 66 to col. 4-line 61). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Satoshi et al. modified by Yamazaki and Mukai so as to include the tapered gate electrode and channel structure of Han et al. because this allows for more tailoring of the device to overcome short channel effects.

Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Satoshi et al., JP 04-139727 in view of Yamazaki, U.S. Patent 4,727,044 and further in view of Mukai, U.S. Patent 5,077,233 and Han et al., U.S. Patent 4,599,118 as applied to claims 18, 21-22, 27, 47, 76, and 89 above, and further in view of Ito et al., "Thin Film Technology of VLSI", pages 87-88.

Satoshi et al., Yamazaki, Mukai and Han et al. are applied as above but both references fail to expressly disclose forming the insulating film using TEOS.

Ito et al. discloses forming an oxide layer using TEOS (see abstract, section 3.3.3). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Satoshi et al. modified by Yamazaki, Mukai and Han so as to form the oxide insulating film using a TEOS precursor because Ito et al. shows this to be a suitable method to form an oxide film.

Claims 16, 19, 29-31, 33, 41-43, 49, 52, 58, 60-61, 68, 78, 81, 84, 87, 93, and 96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoshi et al., JP 04-139727 in view of Yamazaki, U.S. Patent 4,727,044 and further in view of Mukai, U.S. Patent 5,077,233 as applied to claims 12, 15, 17, 23, 26, 28, 34-36, 46, 48, 50, 75, 77, 79, 88, and 90-91 above, and further in view of Chang, U.S. Patent 5,064,775 and Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology".

Satoshi et al., Yamazaki, and Mukai are applied as above but fail to expressly disclose introducing boron into at least a portion of said semiconductor film through said insulating film, said portion to become a channel formation region.

Chang discloses introducing boron 36 into a semiconductor layer so that the boron implanted region becomes part of a channel region (see Fig. 2 and col. 4-line 55 to col. 5-line 37). Furthermore, Wolf et al. discloses that commonly in order to reduce damage to the semiconductor surface, layers are deliberately added, for instance, silicon oxide layers (see page 323, "Implanting Through Surface Layers"). In view of these disclosures, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify the process of Satoshi et al. modified by Yamazaki and Mukai so as to implant boron into the channel region through the silicon oxide insulating film of Mukai because this will allow for more independent control of the threshold voltage.

With respect to forming two active matrix panels and then performing a cutting process, the examiner takes official notice that is a well known method in which to form liquid crystal display devices.

Claims 24, 55-57, 71, 83, 86, and 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoshi et al., JP 04-139727 in view of Yamazaki, U.S. Patent 4,727,044 and further in view of Mukai, U.S. Patent 5,077,233 and Chang, U.S. Patent 5,064,775 and Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology" as applied to claims 16, 19, 29-31, 33, 41-43, 49, 52, 58, 60-61, 68, 78, 81, 84, 87, 93, and 96 above, and further in view of Ito et al., "Thin Film Technology of VLSI", pages 87-88.

Satoshi et al., Yamazaki, Mukai, Chang, and Wolf et al. are applied as above but both references fail to expressly disclose forming the insulating film using TEOS.

Ito et al. discloses forming an oxide layer using TEOS (see abstract, section 3.3.3). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Satoshi et al. modified by Yamazaki and Mukai and Chang and Wolf so as to form the oxide insulating

film using a TEOS precursor because Ito et al. shows this to be a suitable method to form an oxide film.

Claims 13, 37-40, 51, 80, and 92 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoshi et al., JP 04-139727 in view of Yamazaki, U.S. Patent 4,727,044 and further in view of Mukai, U.S. Patent 5,077,233 and Chang, U.S. Patent 5,064,775 and Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology" as applied to claims 16, 19, 29-31, 33, 41-43, 49, 52, 58, 60-61, 68, 78, 81, 84, 87, 93, and 96 above, and further in view of Han et al., U.S. Patent 4,599,118.

Satoshi et al., Yamazaki, Mukai, Chang, and Wolf et al. are applied as above but fail to expressly disclose forming a gate electrode having tapered side edges formed by wet etching and wherein said channel formation region between said source and drain region has a first length in contact with said gate insulating film and a second length at a surface in contact with said insulating surface, where said first length is shorter than said second length.

Han et al. discloses forming a gate electrode with tapered sides which will inherently lead to the channel structure claimed by applicant (see Figures 4-7 and col. 3-line 66 to col. 4-line 61). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Satoshi et al. modified by Yamazaki and Mukai and Chang and Wolf so as to include the tapered gate electrode and channel structure of Han et al. because this allows for more tailoring of the device to overcome short channel effects.

Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over Satoshi et al., JP 04-139727 in view of Yamazaki, U.S. Patent 4,727,044 and further in view of Mukai, U.S. Patent 5,077,233 Chang, U.S. Patent 5,064,775 and Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology and Han et al., U.S. Patent 4,599,118 as applied to claims 13, 37-40, 51, 80, and 92 above, and further in view of Ito et al., "Thin Film Technology of VLSI", pages 87-88.

Yamazaki, Mukai, Chang, Wolf, and Han et al. are applied as above but both references fail to expressly disclose forming the insulating film using TEOS.

Ito et al. discloses forming an oxide layer using TEOS (see abstract, section 3.3.3). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yamazaki modified by Mukai, Chang, Wolf, and Han et al. so as to form the oxide insulating film using a TEOS precursor because Ito et al. shows this to be a suitable method to form an oxide film.

Response to Arguments

Applicant's arguments with respect to claims 12-13, 15-19, 21-24, 26-43, 46-58, 60-61, 65-71, and 75-96 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Richard A. Booth
Primary Examiner
Art Unit 2812